REMARKS

Reconsideration and allowance of this application, as amended, is respectfully requested.

This amendment is in response to the Office Action dated October 31, 2003. By the present amendment, the claims have been amended to clarify the invention. In particular, claims 9 and 32 have been amended to respond to the 35 U.S.C. § 112, second paragraph, rejection set forth in paragraph 3 of the Office Action. Specifically, the words "second" has been removed in claim 9 with regard to the register since no previous register had been defined. Claim 32 has been amended to clarify the relationship of the claim structure to a cache memory. For these reasons, reconsideration and removal of the 35 U.S.C. § 112, second paragraph, rejection is respectfully requested.

Appreciation is expressed for the indication of allowable subject matter in claims 8, 9 and 36. With regard to this, it is respectfully submitted that the parent claims for these claims are in condition for allowance, for reasons which will be discussed below. Accordingly, these claims have not been rewritten into independent format at the present time.

Reconsideration and removal of the 35 U.S.C. § 102(b) rejection of claims 1-7, 10, 32-35, 37-38, 52 and 54-56 over U.S. Patent 5619408 to Black is respectfully requested for reasons set forth below.

Briefly, the present invention is directed to an arrangement for reducing power consumption using an additional circuit to decrease power consumption in data base sections and control sections, such as decoders (e.g. see the last paragraph of page 4). The present invention operates such that, when an unrelated instruction is input

from a cache memory to a discrimination circuit (that is, unrelated to an instruction to perform calculations in a processing circuit), switching in the decoder is decreased, with a resulting decrease in transistor switching. This serves to decrease the through current in the transistors, correspondingly lowering the power consumption of the decoder (e.g., see page 5, line 8 et seq.).

By the present amendment, the independent claims 1, 32 and 52 have each been amended to clarify the distinctions of the present invention over the Black reference. To this end, referring to claim 1 as an example, a cache memory is defined in conjunction with an instruction processor, an instruction decoder to decode the output of the instruction processor and a processor to make calculations according to the output from the instruction decoder. When instructions are input to the instruction processor from the cache memory that are specified instructions, the instruction processor will output the instructions to the instruction decoder. On the other hand, when instructions are input which are other than the specified instructions, a first instruction different from the input instruction is output from the instruction processor to the instruction decoder. Thus, a clear relationship is defined between the cache memory, the instruction processor and the instruction decoder which depends on the contents of the input instructions to the instruction coder from the cache memory.

It is respectfully submitted that Black fails to teach or suggest this claimed relationship between a cache memory, an instructions processor, an instruction decoder and a processor. In particular, Black teaches an IDR logic circuit 46 that recodes each of the three noneffective instructions into a non-op instruction format, as discussed in column 6, line 40 et seq. As shown in Fig. 4, the IDS logic 46

receives an input from a bus interface unit 44. The IDR logic circuit 46 proceeds to provide output instructions to an information cache circuit 48. As such, in Black, the IDR logic circuit 46 provides an output of a changed instruction to an instruction cache circuit 48, unlike the present invention defined by the present claims in which the instruction processor outputs a changed instruction to the instruction decoder. As such, it is respectfully submitted that the independent claims 1, 32 and 52 clearly define a different structure than that set forth in Black, and reconsideration and removal of the rejection based on Black is earnestly solicited.

In the Office Action, the elements of Fig. 2 of the Black reference are indicated as being equivalent to the elements of claim 1 of the present application. In particular, it is stated that the instruction processor outputting the first instruction different from the input instruction to a instruction decoder can be read on column 3, line 41 et seq. of Black. However, it should be noted that Black sets forth in column 3, line 24 et seq. that:

> "A source of inefficiency within an instruction processing subsystems that is unaddressed by either of the prior art systems depicted in Figs. 1 and 2 is the utilization of processor cycle time to execute instructions which do not alter the state of the processor."

Black goes on to state that it would be desirable to replace the instruction that does not effect the state of the processor to a no-op instruction (e.g. see column 3, line 37 et seq.). As such, it is respectfully submitted that the instruction processor defined in claim 1 is quite lacking from the arrangement of Black. This is particularly the case following the amendments to claim 1 which define a relationship between the cache memory and the instruction processor, as well as the claimed relationship between the instructions processor and the instruction decoder. Therefore, reconsideration

and allowance of the amended independent claims 1, 32 and 52 over the cited reference to Black, together with their respective dependent claims, is respectfully requested.

If the Examiner believes that there are any other points which may be clarified or otherwise disposed of either by telephone discussion or by personal interview, the Examiner is invited to contact Applicants' undersigned attorney at the number indicated below.

To the extent necessary, Applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Antonelli, Terry, Stout & Kraus, LLP Deposit Account No. 01-2135 (Docket No. 501.38642X00), and please credit any excess fees to such Deposit Account.

Respectfully submitted,

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